Faculty Development Program

on

Analog Signal Processing and VLSI

(July 13 - 18, 2015)



Organized by

Department of Electronics & Communication Engineering

Jaypee Institute of Information Technology, Noida (Declared Deemed to be University under Section 3 of UGC Act 1956)

About the Institute

Jaypee Institute of Information Technology (JIIT), Noida was established in the year 2001 and has been declared as a "Deemed to be University" under Section 3 of UGC Act 1956. The institute was founded by revered Shri Jaiprakash Gaur ji and is run by Jaypee Sewa Sansthan with a vision to become a Centre of Excellence comparable to the best in the world for producing professionals with leadership quality in technology, innovation, entrepreneurship and management. The undergraduate programs of the university have been accredited by the National Board of Accreditation of AICTE. Well equipped modern laboratories and an intellectually stocked Learning Resource Centre provide a pleasant and stimulating ambience.

The Electronics and Communication Engineering department was formed in the year 2002. Besides running a 4 year B. Tech degree and 5 years Integrated B.Tech-M.Tech degree program in Electronics Communication Engineering, the department is also running two M.Tech degree program with specialization in Communication System (CS) and Microelectronics and Embedded Technology (MET) and PhD program in all

key areas of electronics. The department is actively involved in research in the areas of Emerging Communication Technologies, Current-mode Analog Signal Processing, Digital Signal Processing, Image Processing, Microwave Engineering, VLSI Design, MEMS. Wireless communication etc.

Scope of the Program

The aim of this program is to provide an exposure to the concept of analog circuit design using current-mode approach which suits low voltage low power analog signal processing applications. This program will introduce new innovative and interesting methods of teaching and learning subjects like low voltage low power analog circuit design and concepts of VLSI design through a series of talks and practical. Following topics will be covered in the FDP:

- Signal Processing
- **Current Conveyors and their Variants**
- **High Performance Active Devices**
- **CCCCTA** as Electronic Tunable active element.
- **ECSM Characterization of CMOS Inverter**
- **Image Processing**
- Hands on Laboratory course on Cadence Virtuoso
- SPICE and Circuit Simulation Lab.

Speakers

- 1. Prof. Hariom Gupta (Director, JIIT, Sec. 128, Noida)
- 2.Dr. Shweta Srivastava (Department of ECE, JIIT, Noida)
- 3. Dr. Sajai Vir Singh (Department of ECE, JIIT, Noida)
- **4.Dr.** Jitendra Mohan (Department of ECE, JIIT, Noida)
- 5. Dr. Bhartendu Chaturvedi (Department of ECE, JIIT Noida)
- **6. Dr. Megha Agarwal** (Department of ECE, JIIT, Noida)
- 7. Dr. Madhu Jain (Department of ECE, JIIT, Noida)
- **8. Ms. Baljit Kaur** (Department of ECE, JIIT, Noida)

Who should attend?

is open program to all faculty The members/scientists/engineers working in educational institutes/industries/R & D Organizations.

Duration and Venue

FDP will be held at: JIIT, Sector-128 campus, Jaypee Wish Town, Sector-128, NOIDA from 13th -18th July.

2015. Last date to receive duly filled registration forms of applicants is **July 7, 2015**.

Registration Details

Registration fee: Rs. 2000/- The fee includes lunch and tea during the program. No TA/DA or Boarding will be provided. Registration fees can be paid by Demand Draft (DD), in favor of "Jaypee Institute of Information Technology", payable at NOIDA which may be sent to the following address along with the registration form and a passport size photograph of the applicant. For more info please visit www.jiit.ac.in.

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REGISTRATION FORM

NAME	:
Academic Qualification:	
Designation	:
Department	:
Organization	:
Address (O)	:
Phone/Fax	:
Email	:
Payment Details (DD No./:Transaction No. etc)	

Signature of the Participant